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Attention: Dr. Francis J. Kub
Subject: Monthly Progress Report - April 1997
Reference: SiGe Power HBT

Gentlemen:

1.0 Introduction

The objective of this program is the development and demonstration of a viable SiGe power HBT device design and associated processes that will demonstrate >1 Watt of output power at 6 and 8 GHz.

2.0 Objectives for the Reporting Period

2.1 Complete wafer processing of the SiGe2 and BUR50 designs which utilize the NiCr thin film ballast resistors.

2.2 Complete wafer processing of the UHVCVD epitaxial system deposition wafer lot of SiGe2 design (see Section 5.1)

2.3 Continue device evaluation at PHO and at CR&D.

3.0 Progress During the Reporting Period

3.1 The run of the SiGe2 design targeted for NiCr ballasting, which was started utilizing the NRL previous collector epitaxial designs, have completed wafer fabrication, 100% DC probing, and dicing as single cell die. These wafers are presently undergoing RF evaluation at both CR&D and PHO.

3.2 The run of the BUR50 design targeted for NiCr ballasting, which was started simultaneously with the SiGe2 design, has been required to be reworked through metallization including the deposition of the NiCr resistors. This was caused by a

defect in the Metal-1 photomask and unfortunately was not observed until after Metal-1 liftoff.

3.3 Photomasks for the alternate approach which forms the ballast resistors from polycrystalline silicon and has been applied to the **SiGe2** design were received in early March.

This wafer run utilizing this design approach has completed Selective SiGe Base Epitaxial Growth, PolyRes Photo & Etch, BV_{cbo} Measurement, PCM Measurement, LTO Deposition, EBC Photo & Etch, UHVCVD Polysilicon Deposition, Phosphorous Implant is awaiting Polysilicon Emitter Photo.

The surface quality resulting from the selective SiGe epitaxial growth exhibited a highly faulted/hillock condition in the expected single crystal areas. However, the BV_{cbo} measurements which were performed in key areas indicated approximately 28 volt and 40 volt collector-base breakdown on the two respective collector epitaxial layers. This is well within the expected limits for final device operation under common base operation at 10 and 20 volts respectively.

3.4 In order to try to improve the consistency of the contact resistance associated with the formation of the polysilicon emitter, a **SiGe2** design wafer run has been intiated into the BSO fab. This run utilizes the **UHVCVD epitaxial** system to deposit the polysilicon layer. This run has completed wafer fabrication, 100% DC probing, and dicing. This run is presently undergoing assembly for RF characterization.

3.5 The design of **SiGe3**, which is a pizza mask approach aimed at establishing a design library for SiGe power transistor structures, has been completed. Initial photomasks from the vendor were received on 4/23/97 and the initial design run has been initiated into the wafer fab.

3.6 There was no significant device testing at CR&D during this period due to a defective 6 GHz power amplifier in the load-pull test system.

5.0 Problems and Proposed Solutions

(See above description.)

5.0 Objectives for the Next Reporting Period

5.1 Continue processing of the **pizza mask SiGe3** wafer run.

5.2 Perform RF characterization of the **UHVCVD epitaxial SiGe2** wafer run.

5.3 Complete processing of the **polysilicon ballast SiGe2** wafer run.

5.4 Complete rework processing of the **thin film resistor ballast BUR50** wafer lot.

5.5 Perform RF evaluation of the **thin film resistor ballast SiGe2** wafer lot.

Respectfully,

M/A-COM Inc.

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